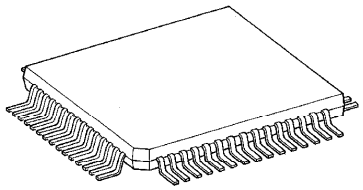
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T9947S, JT9947X-AS

T9947S, JT9947X-AS CMOS SINGLE-CHIP LSI FOR LCD CALCULATOR

The T9947S, JT9947X-AS is a single-chip microcomputer for 10-digit 1-memory electronic calculator.
T9947S, JT9947X-AS can drive the liquid crystal display (LCD). Single power supply operation, low-power consumption make it suitable for solar battery or battery operated pocketable calculator.



LQFP60-P-1414-0.80

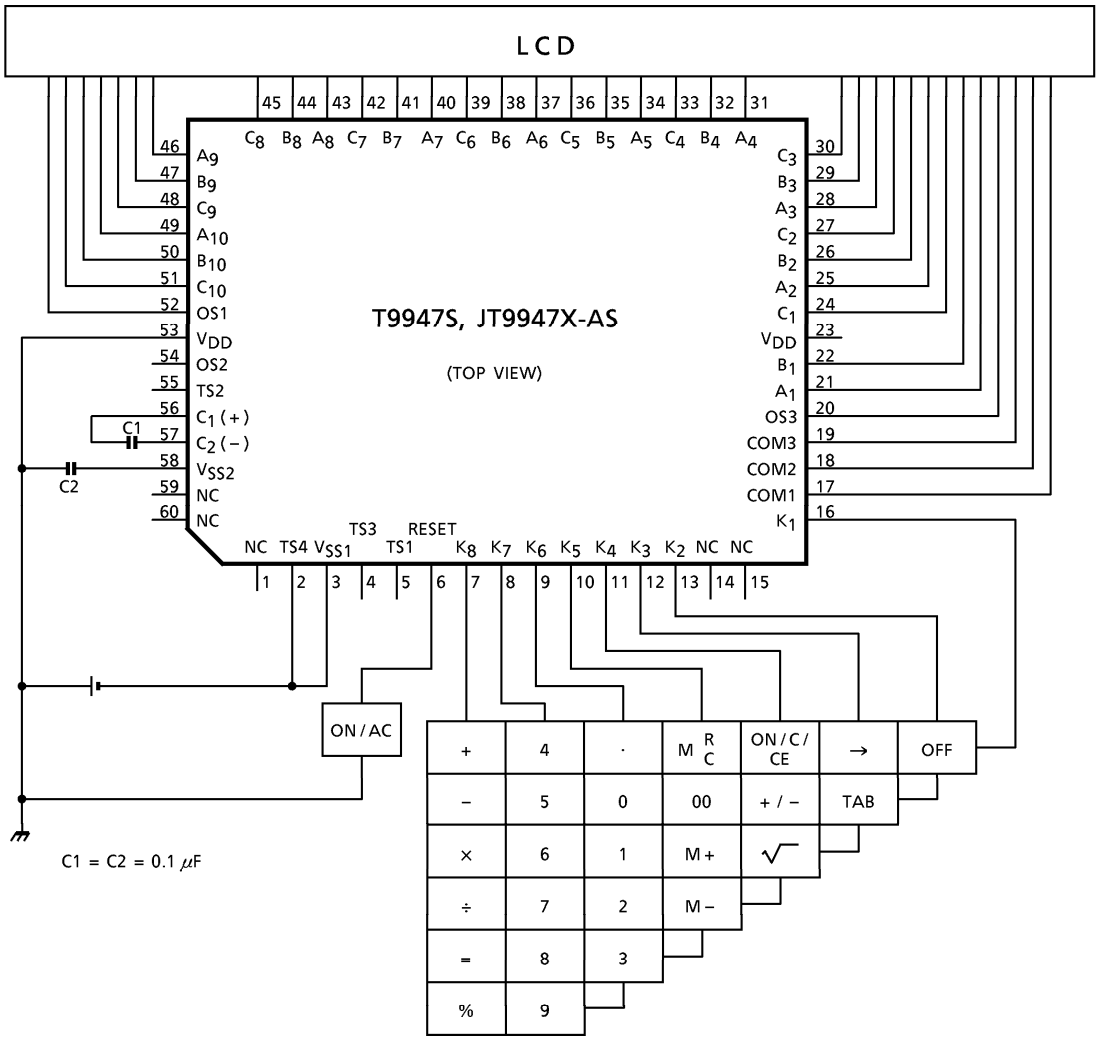
Weight : 0.66 g (Typ.)

FEATURES

- 10 digits of data and 1 symbol digit for calculator.
- Algebraic calculation mode.
- Punctuation.
- Standard 4 functions (+, −, ×, ÷), square root, percent with automatic add-on / discount, automatic constant calculations, chain calculations, memory calculations with memory overflow protection.
- Internal keyboard decoding and denouncing.
- Complementary output buffer for direct driving of liquid crystal display (LCD : FEM type −3.0 V, 1 / 2 bias, 1 / 3 duty).
- Single power supply (−1.5 V typ.).
- Quad in line flat package (60 pin).
- Very low power consumption (3.0 μW typ. at wait).
- Very wide range of operating voltage (V_{SS1} = −1.2~−2.0 V).

SYSTEM BLOCK DIAGRAM

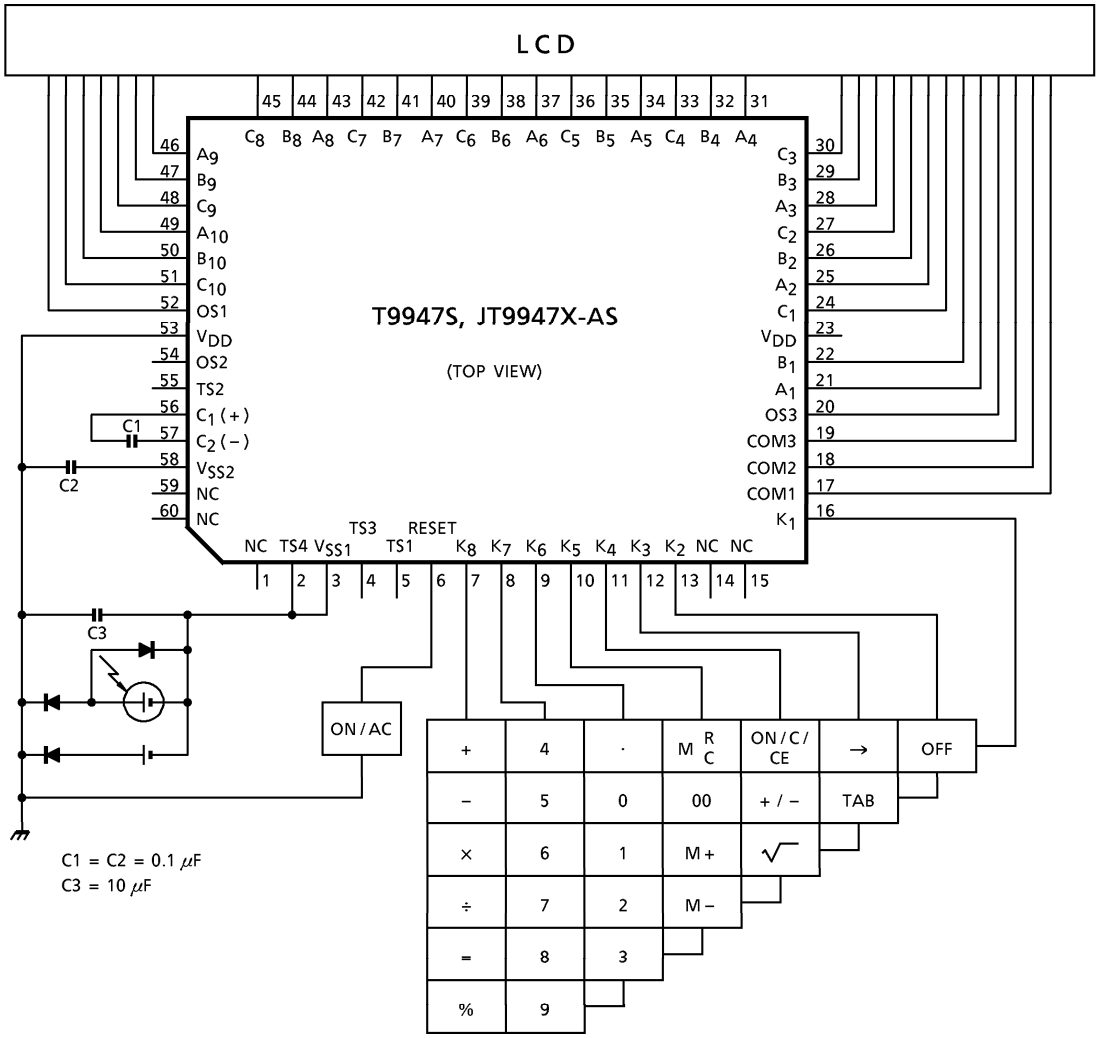
Battery Type



(Note) : TS4 { V_{DD} ……OFF MODE DISABLE
V_{SS1} ……OFF MODE ENABLE

Solar Capacitor C3 ≦ 10 μF
Rkey ≦ 20 kΩ (– 1.2 V)
≦ 135 kΩ (– 1.5 V)

Dual Type



(Note) : TS4 { V_{DD} ……OFF MODE DISABLE
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Solar Capacitor C3 ≦ 10 μF
Rkey ≦ 20 kΩ (– 1.2 V)
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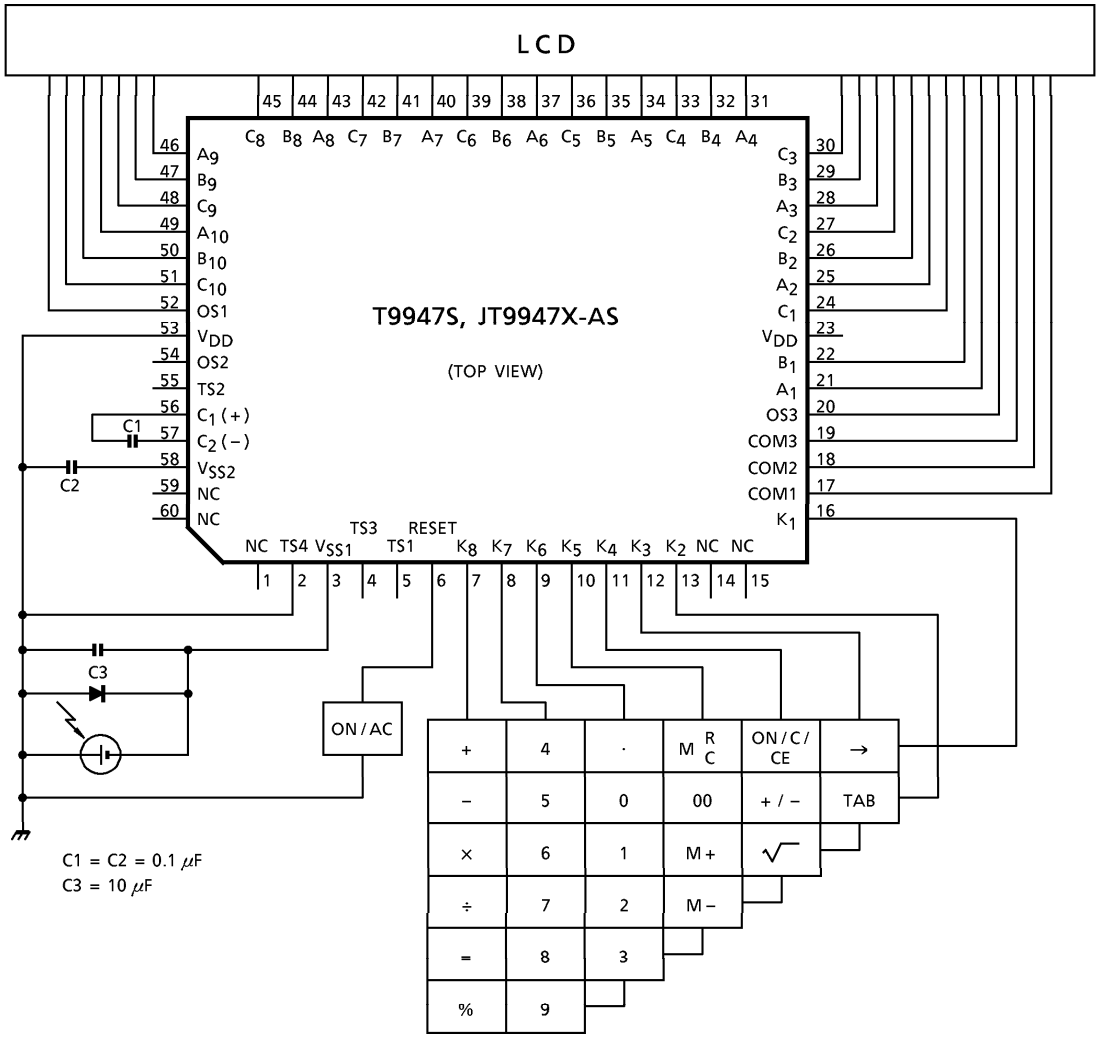
Solar Type

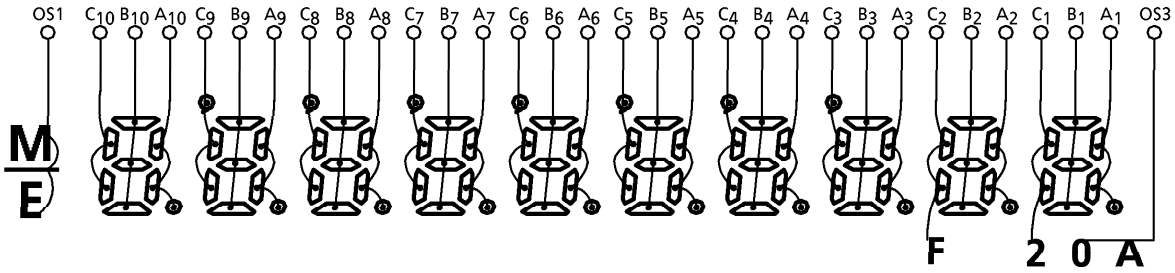


(Note) : TS4 { V_{DD} ……OFF MODE DISABLE
V_{SS1} ……OFF MODE ENABLE

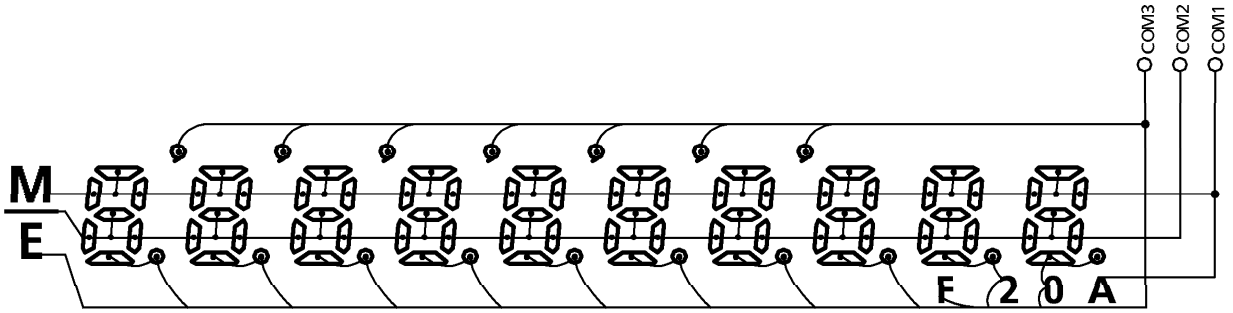
Solar Capacitor C3 ≦ 10 μF
Rkey ≦ 20 kΩ (– 1.2 V)
≦ 135 kΩ (– 1.5 V)

CONNECTION OF LCD

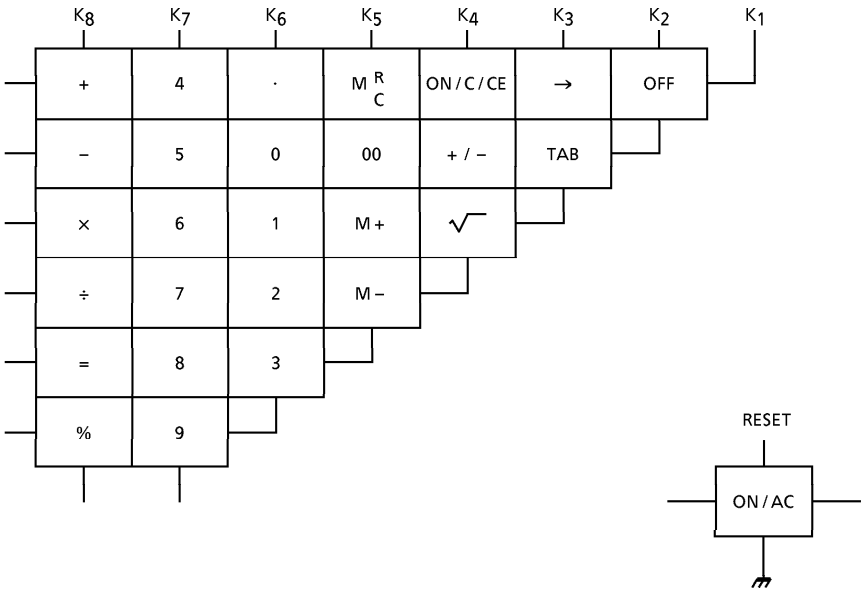
SEGMENT



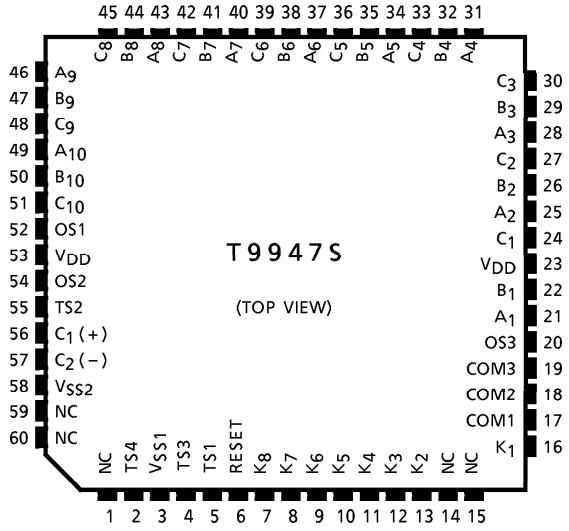
COMMON



KEY CONNECTION



PIN ASSIGNMENT



SPECIFICATION OF CALCULATOR

Operational Features

(1) 10 digits of data and 1 symbol digit.

(2) Algebraic mode.

(3) Full floating point.

(4) Standard 4 functions +, −, ×, ÷.

(5) Memory calculation.

(6) Square root.

(7) Percent with automatic add-on and discount.

(8) Constant calculation (Automatic constant).

(9) Chain calculation.

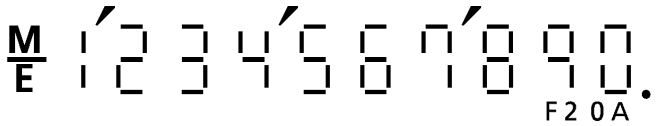
(10) Leading zero suppression.

(11) Trailing zero suppression.

Capacity of Calculation

(1)	Numeral entry	10 digits
(2)	Addition / Subtraction	10 digits + (−) 10 digits = 10 digits
(3)	Multiplication / Division	10 digits × (÷) 10 digits = 10 digits
(4)	Memory calculation	10 digits + (−) 10 digits = 10 digits
(5)	Square root	$\sqrt{10}$ digits = 10 digits

Display Font



Overflow Condition

(1) When division by zero is attempted, an overflow condition will result, and error symbol "E" and a zero are displayed.

(2) When the integer part of result exceeds 10 digits, the display will show 10 most significant digits of result divided by 10^{+10} and "E".

(3) When the integer part of result exceeds 19 digits, display will show a zero and "E".

(4) When the integer part of result in memory register exceeds 10 digits at memory calculation, display will show a zero and "E", and previous data will be kept in memory resister.

(5) When an overflow occurs on the way of add-on / discount calculation, display will show a zero and "E".

(6) When square root of any negative number is attempted, "E" and square root of absolute value are displayed.

(7) In overflow condition, any operation or numeral entry will be inhibited.

Clearing Overflow Condition

(1) The resulting overflow condition can be cleared by depressing [ON / C / CE] .

(2) At memory overflow condition, depression of [MRC] after [ON / C / CE] will recall the previous memory data.

(3) At the condition of exceeding capacity overflow occurred in chain calculation, depression of [ON / C / CE] will reset the error symbol "E", and you can continue the calculation using the displayed data.

Speed of Calculation

(1)	Numeral entry					74.4 ms
(2)	Addition	1111111111	+	1111111111	=	102.7 ms
(3)	Multiplication	1	×	9999999999	=	394.7 ms
(4)	Division	9999999999	÷	1	=	394.7 ms
(5)	Memory calculation	9999999999	÷	1	M+	482.7 ms
(6)	Percentage calculation	1	+	9999999999	%	378.7 ms
(7)	Square root			9999999999	√	326.7 ms

Keys for Calculator

(1) Data Keys

The data keys consist of numeral keys 0 , 00 through 9 and a decimal point key · . The first of a sequence of data keys will clear the contents of display register before being entered. The decimal point key will be accepted the first time it is depressed during calculations.

(2) Arithmetic Operation Keys

The arithmetic operation keys include the plus + , minus − , multiply × , divide ÷ , equal = , percent % , square root √ , memory add M+ , memory subtract M− , sign change +/− , data shift →.

+ Depression of this key conditions the calculator for addition of display register to upper register.
If the calculator was previously conditioned for add, subtract, multiply or device, those operation would be performed with the resultant intermediate sum, difference, product or quotient displayed and previous modes and reset, and calculator stores add command.
In the successive depressions of this key, the first will perform the previously enabled mode and more than twice depressions will be ignored.

− Depression of this key performs the same function as the + key with the exception that calculator stores subtract mode.

× Depression of this key conditions the calculator for multiplication of upper register and display register.
If the calculator was previously conditioned for add, subtract multiply or divide, those operation would be performed with the resultant intermediate sum, difference, product or quotient displayed.
And then set the multiply mode.

[M −] Depression of this key will perform the same function as the [M +] with the exception that the calculator result or displayed number is subtracted from the memory register.

[=] Depression of this key following numeral entry will perform the previously enabled mode.
If no number has been entered, the displayed number will be used to perform the previously enabled mode. If no mode are enabled, this key will be ignored. If multiplication or division are enabled, constant mode operations are performed by termination a sequence of operations with the [=] key, entering a new number and depressing the [=] key.
Any key sequence terminated with, [=] key will not require the use of [ON / C / CE] key before a new operation sequence can be initiated.

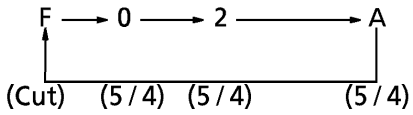
[%] If the calculator was previously conditioned for addition, or subtraction or multiplication or divination, [%] calculations would be performed as follows.

a + b [%] a + a·b / 100
a − b [%] a − a·b / 100
a × b [%] a·b / 100
a ÷ b [%] 100 a / b

If no mode are enabled, this key will be ignored. If multiplication or division are enabled, constant mode operations are performed by terminating a sequence of operation with the [%] key, entering new number and depressing the [%] key.

[M +] Depression of this key will perform the previously enabled mode and add the result to memory register and leave the result in the display register.
If no modes are enabled, the displayed number is added to memory register by this key.
Any key sequence terminated with [M +] will not require the use of the [ON·/ C / CE] key before a new operation sequence can be initiated.

[TAB] "TAB" fixed point mode selectable



[÷] Depression of this key performs a similar function as the [×] key except that division of upper register by display register is either set up or performed and the divide mode is activated.

[√] Depression of this key calculated the square root of number displayed without changing modes of operation.
Depression of this key following [+], [−], [×], or [÷] keys will transfer the contents of display register to upper register and calculate the square root of number displayed.
The entry of a new number following this key clear the previous display.

[+ / −] Depression of this key will change the sign of display register.

[→] Depression of this key will shift the right data of display register.

(3) Command Function Keys

The command function keys include the clear entry / clear all [ON / C / CE], recall / clear memory [MRC]

[MRC] Depression of this key following [+], [−], [×] or [÷] will transfer the contents of display register to upper register and recall the contents of memory register to display register.
[MRC] key following [=], [%], [M+], [M−] or any number key will recall the contents of memory register to the display register without affecting any other operations in progress.
Successive depressions of [MRC] key will clear the memory register.

[ON / C / CE] Depression of this key after [MRC], [√], [·], or numeral keys will clear the display register.
You can reset the error symbol "E" if you depress [ON / C / CE] at the condition of exceeding capacity error.

[OFF] Depression of this key will off the LSI.

Arithmetic Operations

1. Addition

Key Op.	Display
A	A
[+]	A
B	B
[+]	A + B
C	C
[=]	A + B + C
D	D
[+]	D
E	E

	Key Op.	Display
	[+]	D + E
	[=]	D + E

2. Subtraction

(1)	A	A
	[−]	A
	B	B
	[−]	A − B
	C	C
	[=]	A − B − C
	[−]	A − B − C
	D	D
	[+ / −]	− D
	[−]	A − B − D + D
	[=]	− (A − B − C + D)

3. Multiplication

(1)	A	A
	[×]	A
	B	B
	[=]	A·B
	[+]	A·B
	C	C
	[=]	A·B + C
(2)	[−]	0.
	A	A
	[×]	− A
	B	B
	[=]	− A·B

		Key Op.	Display
4. Division			
	(1)	A	A
		[÷]	A
		B	B
		[=]	A / B
	(2)	[−]	0.
		A	A
		[÷]	− A
		B	B
		[=]	− A / B
5. Power calculation			
	(1)	A	A
		[×]	A
		[=]	A^2
		[=]	A^3
	(2)	A	A
		[÷]	A
		[=]	1 / A
		[=]	$1 / A^2$
	(3)	[−]	0.
		A	A
		[×]	− A
		[=]	A^2
		[=]	$-A^3$
	(4)	[−]	0.
		A	A
		[÷]	− A
		[=]	− 1 / A
		[=]	$1 / A^2$

	Key Op.	Display
(5)	A	A
	[×]	A
	[=]	A^2
	[×]	A^2
	[=]	A^4

6. Mixed calculation

(1)	A	A
	[×]	A
	B	B
	[+]	A·B
	C	C
	[÷]	A·B + C
	D	D
	[−]	$\frac{A \cdot B + C}{D}$
	E	E
	[=]	$\frac{A \cdot B + C}{D} - E$

7. Constant calculation

(1)	A	A
	[×]	A
	B	B
	[=]	A·B
	C	C
	[=]	A·C
(2)	[−]	0.
	A	A
	[×]	− A
	B	B
	[=]	− A·B
	C	C

	Key Op.	Display
	[=]	– A·C
(3)	A	A
	[÷]	A
	B	B
	[=]	A / B
	C	C
	[=]	C / B
	D	D
	[×]	D
	[=]	D^2
(4)	A	A
	[+]	A
	B	B
	[=]	A + B
	C	C
	[=]	C
(5)	A	A
	[−]	A
	B	B
	[=]	A – B
	C	C
	[=]	C
(6)	A	A
	[×]	A
	B	B
	[=]	A·B
	C	C
	[×]	C
	D	D

	Key Op.	Display
	[=]	C·D
	E	E
	[=]	C·E
	[×]	C·E
	F	F
	[=]	C·E·F
	G	G
	[÷]	G
	H	H
	[=]	G / H
	I	I
	[=]	I / H
(7)	A	A
	[×]	A
	B	B
	[%]	A·B / 100
	C	C
	[%]	A·C / 100
	D	D
	[÷]	D
	E	E
	[%]	100·D / E
	F	F
	[%]	100·F / E

8. Mark-up / Discount calculator

(1)	A	A
	[×]	A
	B	B
	[+]	A·B
	[=]	A + A·B

	Key Op.	Display
(2)	A	A
	×	A
	B	B
	−	A·B
	=	A − A·B
(3)	A	A
	×	A
	B	B
	%	A·B / 100
	+	A·B / 100
	=	A + A·B / 100
(4)	A	A
	×	A
	B	B
	%	A·B / 100
	−	A·B / 100
	=	A − A·B / 100
(5)	A	A
	+	A
	B	B
	%	A + A·B / 100
(6)	A	A
	−	A
	B	B
	%	A − A·B / 100

9. Memory calculation

	Key Op.	Display	Memory
(1)	A	A	0.
	M +	A (M)	A
	B	B (M)	A

	Key Op.	Display	Memory
	[M+]	B (M)	A + B
	C	C (M)	APB
	[M−]	C (M)	A + B − C
	D	D (M)	A + B − C
	[MRC]	A + B − C (M)	A + B − C
	MRC	A + B − C	0.
(2)	A	A	0.
	[+]	A	0.
	B	B	0.
	[M+]	A + B (M)	A + B
	[+]	A + B (M)	A + B
	[M+]	A + B (M)	2 (A + B)
	C	C (M)	2 (A + B)
	[M−]	C (M)	2 (A + B) − C
(3)	A	A	0.
	[×]	A	0.
	B	B	0.
	[M+]	A·B (M)	A·B
	C	C (M)	A·B
	[×]	C (M)	A·B
	D	D (M)	A·B
	[M−]	C·D (M)	A·B − C·D
	[MRC]	A·B − D·D (M)	A·B − C·D
	[M−]	A·B − C·D	0.
(4)	A	A	0.
	[×]	A	0.
	B	B	0.
	[=]	A·B	0.
	C	C	0.
	[M+]	C (M)	C

	Key Op.	Display	Memory
	[=]	A·C (M)	C
	D	D (M)	C
	[M −]	D (M)	C − D
	[=]	A·D (M)	C − D
(5)	A	A	0.
	[M +]	A (M)	A
	B	B (M)	A
	[M +]	B (M)	A + B
	[MRC]	A + B (M)	A + B
	×	A + B (M)	A + B
	[MRC]	A + B (M)	A + B
	[+]	$(A + B)^2$ (M)	A + B
	C	C (M)	A + B
	[=]	$(A + B)^2 + C$ (M)	A + B
(6)	1.000000001	1.000000001	0.
	M +	1.000000001 (M)	1.000000001
	9999999999	9999999999. (M)	1.000000001
	[M +]	0. ($_{E}^{M}$)	1.000000001
	[ON / C / CE]	0. (M)	1.000000001
	[MRC]	1.000000001 (M)	1.000000001

10.Square root

(1)	A	A	
	[√]	$\sqrt{A}$	
	B	B	
(2)	A	A	
	[×]	A	
	B	B	
	[√]	$\sqrt{B}$	
	[=]	$A\sqrt{B}$	

	Key Op.	Display	Memory
(3)	A	A	
	×	A	
	√	√A	
	B	B	
	=	A·B	
(4)	−	0.	
	A	A	
	=	− A	
	√	√A (E)	
(5)	A	A	0.
	M+	A (M)	A
	MRC	A (M)	A
	÷	A (M)	A
	B	B (M)	A
	+/−	− B (M)	A
	√	√B (ME)	A
	ON/C/CE	0. (M)	A

11. Percentage calculation

(1)	A	A	
	×	A	
	B	B	
	%	A·B / 100	
	C	C	
	%	A·C / 100	
	D	D	
	%	A·D / 100	
(2)	A	A	
	%	A	
	B	B	

	Key Op.	Display	Memory
	[%]	B	
	C	C	
	[%]	C	
(3)	A	A	
	[−]	A	
	B	B	
	[%]	A − A·B / 100	
	[−]	A − A·B / 100	
	[+]	A − A·B / 100	
	C	C	
	[%]	$\left(A - \frac{A \cdot B}{100}\right) + \frac{\left(A - \frac{A \cdot B}{100}\right) \cdot C}{100}$	

12. Key correction

(1)	A	A	0.
	[×]	A	0.
	[÷]	A	0.
	[−]	A	0.
	[+]	A	0.
	[√]	$\sqrt{A}$	0.
	[M+]	A + $\sqrt{A}$ (M)	A + $\sqrt{A}$
	[+/−]	− (A + $\sqrt{A}$) (M)	A + $\sqrt{A}$
	[MRC]	A + $\sqrt{A}$ (M)	A + $\sqrt{A}$
	[MRC]	A + $\sqrt{A}$	0.
	B	B	0.
	[+]	B	0.
	[−]	B	0.
	[×]	B	0.
	[÷]	B	0.
	[=]	1 / B	0.

13. Others		Key Op.	Display	Memory
	(1)	A	A	
		[+]	A	
		[=]	A	
	(2)	A	A	
		[×]	A	
		[÷]	A	
		[=]	1 / A	
	(3)	A	A	
		[%]	A	
		[+]	A	
		[=]	A	
	(4)	A	A	
		[×]	A	
		[−]	A	
		[=]	− A	
	(5)	A	A	
		[÷]	A	
		[−]	A	
		[=]	− A	
	(6)	A	A	
		[×]	A	
		[ON / C / CE]	0.	
		B	B	
		[=]	B	
	(7)	A	A	
		[×]	A	
		B	B	
		[ON / C / CE]	0.	
		C	C	
		[=]	A·C	

Key Chattering Protection

(1) At time of key on : about 18.0 ms, after key input. ($f\phi$ typ.)

(2) At time of key off : about 17.0 ms, after completion of the operation ($f\phi$ typ.)

(3) Simultaneous Keying protection

If 2 or more keys are pressed simultaneously, any key input is not accepted.

MAXIMUM RATINGS

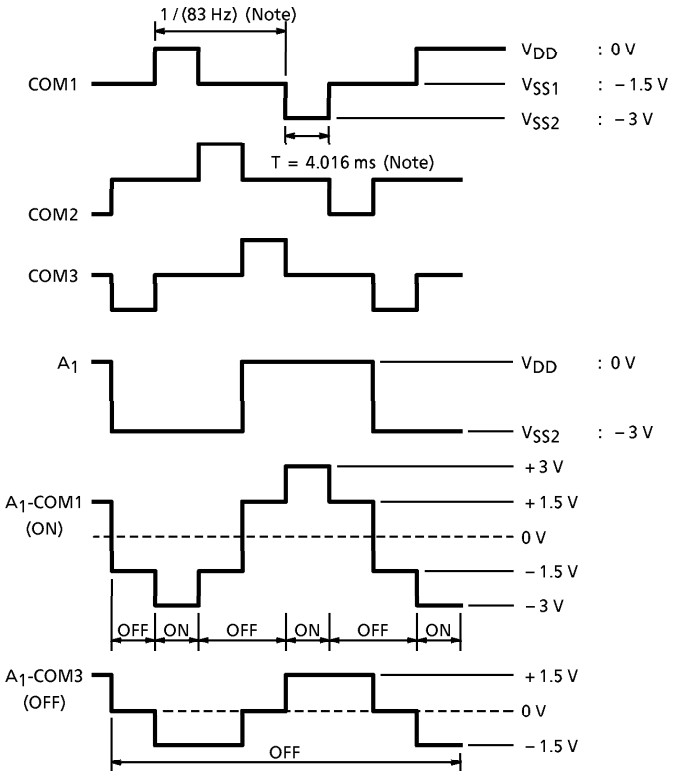
CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	V_{SS1}	+0.3~−2.2	V
Input Voltage	V_{IN}	+0.3~V_{DD1} − 0.3	V
Operating Temperature	T_{opr}	+0.0~40	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (V_{SS1} = −1.5 V ± 0.2 V, V_{SS2} = −3.0 V ± 4.0 V, V_{DD} = 0 V, Ta = 25°C)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage		V_{SS1}	—	—	—	−1.2	−1.5	−2.0	V
VOLTAGE	Input "1"	V_{IH}	—	K_2~K_8, RESET	—	V_{SS1} +0.4	—	V_{SS1}	V
	Input "0"	V_{IL}	—	K_2~K_8, RESET	—	0	—	−0.4	V
	Output "1"	V_{OH}	—	Segment, Common	—	V_{SS2} +0.2	—	V_{SS2}	V
	Output "0"	V_{OL}	—	Segment, Common	—	0	—	−0.2	V
	Output "1"	V_{OH}	—	K_1~K_8, RESET	—	V_{SS1} +0.2	—	V_{SS1}	V
	Output "0"	V_{OL}	—	K_1~K_6, RESET	—	0	—	−0.2	V
Resistance	Output "1"	R_{OH}	—	Segment	V_{OUT} = V_{SS2} + 0.5 V	—	—	70	kΩ
	Output "0"	R_{OL}	—	Segment	V_{OUT} = −0.5 V	—	—	70	kΩ
	Output "1"	R_{OH}	—	Common	V_{OUT} = V_{SS2} + 0.5 V	—	—	70	kΩ
	Output "0"	R_{OL}	—	Common	V_{OUT} = −0.5 V	—	—	70	kΩ
	Pull Up	R_{KH}	—	K_1~K_8	V_{OUT} = 0 V	60	400	1500	kΩ
		RESET	—	RESET	V_{OUT} = 0 V	180	300	420	kΩ
	Output "0"	R_{OL}	—	K_1~K_6	V_{OUT} = −0.5 V	—	—	10	kΩ
Supply Current 1 (On Display)		I_{DD1}	—	—	V_{SS1} = −1.5 V (No Keys)	—	−2.2	−3.6	μA
Supply Current 2 (Operation)		I_{DD2}	—	—	V_{SS1} = −1.2 V (Peak OF A11 9√‾)	—	−4.4	−6.6	μA
Supply Current 3 (Off)		I_{DD3}	—	—	V_{SS1} = −1.5 V (Off Status)	—	−0.5	−2.0	μA
Oscillating Frequency		f_{osc} (WAIT)	—	—	V_{SS1} = −1.5 V, On Display	5.4	9	12.6	kHz
		f_{osc} (OP)			V_{SS1} = −1.5 V, On Operating	10.8	18	25.2	kHz
Frame Frequency		f_F	—	—	V_{SS1} = −1.5 V (Wait)	50	83	117	Hz

WAVEFORMS FOR DISPLAY

Display Device : FEM type LCD −3.0 V, 1/2 bias, 1/3 duty dynamic system



(Note) : f_ϕ = 9 kHz

OTHERS

- AUTO POWER OFF (Typ.) = 7 MIN
- RESET Key

  i) After releasing this key, the cpu is reset and display "0".

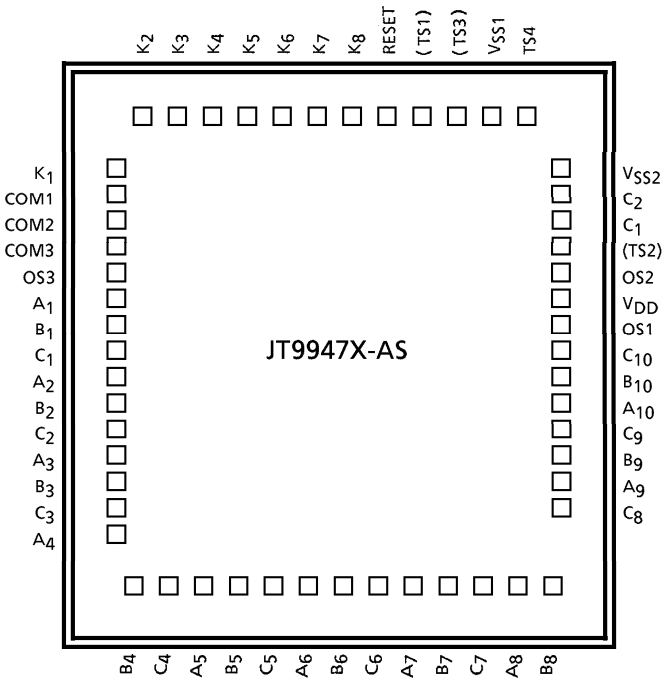
PAD LOCATION TABLE (μm)

NAME	X POINT	Y POINT
K_1	– 1291	1093
COM1	– 1291	896
COM2	– 1291	744
COM3	– 1291	592
OS3	– 1291	441
A_1	– 1291	289
B_1	– 1291	137
C_1	– 1291	– 14
A_2	– 1291	– 166
B_2	– 1291	– 318
C_2	– 1291	– 470
A_3	– 1291	– 621
B_3	– 1291	– 773
C_3	– 1291	– 925
A_4	– 1291	– 1076
B_4	– 927	– 1249
C_4	– 776	– 1249
A_5	– 624	– 1249
B_5	– 472	– 1249
C_5	– 320	– 1249
A_6	– 169	– 1249
B_6	– 17	– 1249
C_6	135	– 1249
A_7	286	– 1249
B_7	438	– 1249
C_7	590	– 1249
A_8	741	– 1249
B_8	893	– 1249
C_8	1254	– 1077

NAME	X POINT	Y POINT
A_9	1254	– 925
B_9	1254	– 774
C_9	1254	– 622
A_{10}	1254	– 470
B_{10}	1254	– 319
C_{10}	1254	– 167
OS1	1254	– 15
V_{DD}	1254	137
OS2	1254	288
(TS2)	1254	489
C_1	1254	697
C_2	1254	898
V_{SS2}	1254	1100
TS4	949	1249
V_{SS1}	798	1249
(TS3)	646	1249
(TS1)	494	1249
RESET	343	1249
K_8	191	1249
K_7	39	1249
K_6	– 112	1249
K_5	– 264	1249
K_4	– 416	1249
K_3	– 568	1249
K_2	– 719	1249

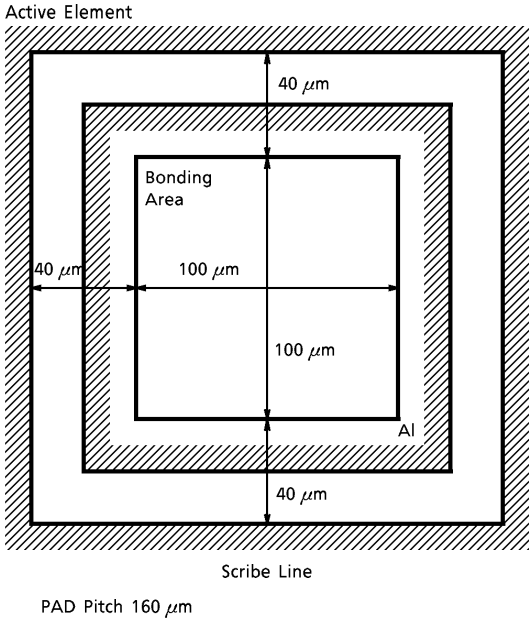
(Note) : ( ) Do not connect.

CHIP LAYOUT



Chip size : 3.04 × 3.02 [mm]
Chip thickness : 290 ± 20 [μm]
Substrate : V_{DD}

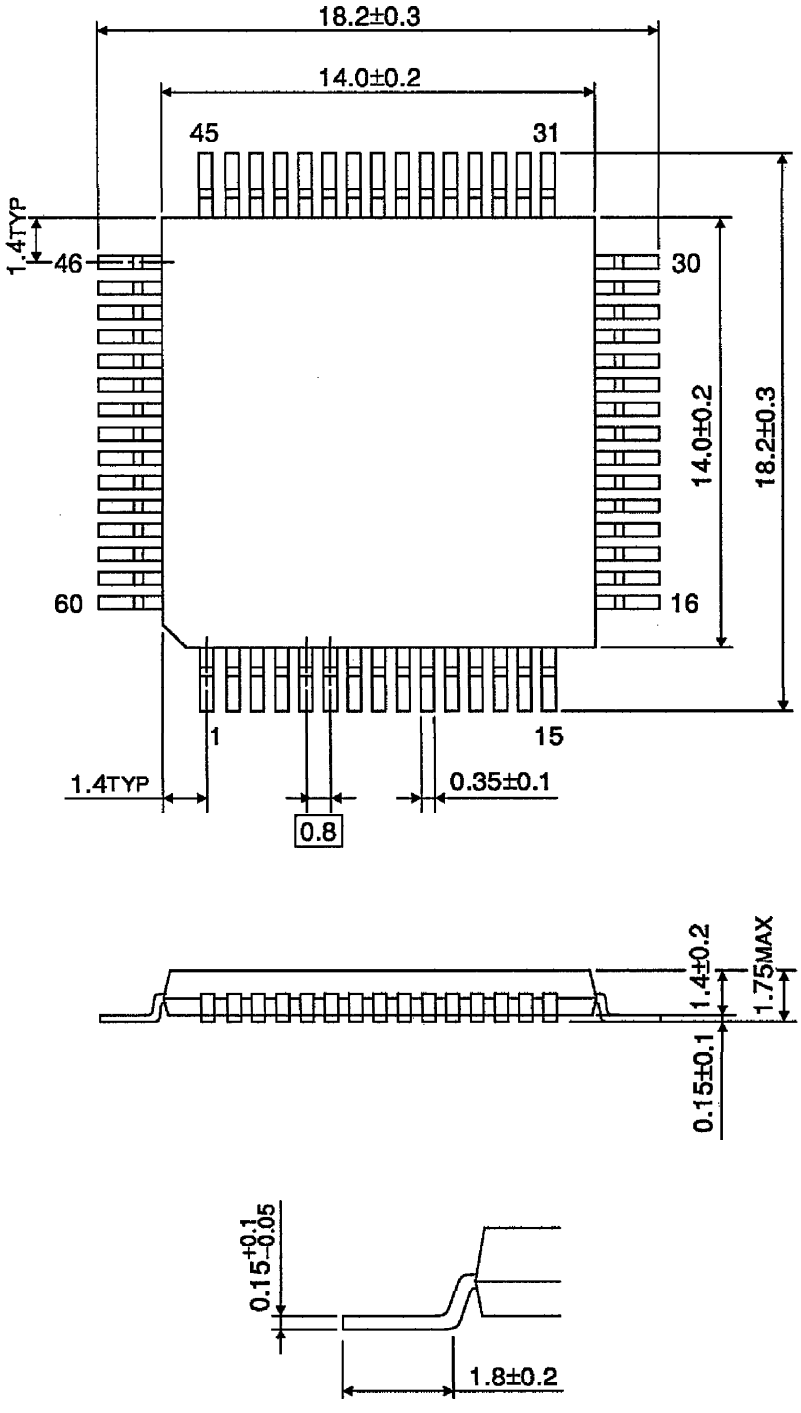
PAD LAYOUT



PAD Pitch 160 μm

PACKAGE DIMENSIONS

LQFP60-P-1414-0.80 Unit : mm



Weight : 0.66 g (Typ.)

General Specification for Bare Calculator LSI Chip

1. Purpose

This is to specify the quality standard for integrated circuits produced by TOSHIBA CORPORATION (hereinafter referred to as VENDOR) which are to be delivered to PURCHASER.

2. Definition

This specification applies only to the bare calculator LSI chips produced by VENDOR and purchased by PURCHASER and defines the general specification items.

3. Priority of specifications

When there are discrepancies in or questions arising from the specifications and instructions provided by VENDOR, the following documents shall apply, in the priority order shown.

1) Individual specifications for the bare calculator LSI chip
(both PURCHASER and VENDOR should refer to the technical data sheet for the relevant product.)
2) General specifications for the bare calculator LSI chip
3) Other related specifications and standards

4. Characteristics

To be shown in the individual specification sheets.
The individual specifications shall consist of the following four items.

1) Rating specifications
2) Electrical characteristics
3) Pin configuration and mechanical dimensions
4) Others

5. Inspection of product for delivery

5.1 Inspection lot

a) The inspection lot shall consist of products produced using the same material, working from the same design, via the same production process, using the same facilities, with the same assured quality and using the same quality assurance method; the lot number shall be put on all trays to allow tracing of the lot history.

b) The products in an inspection lot number should all be taken from the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level Ⅱ.

The acceptable quality level (AQL) shall be as specified in the following table:

TEST	AQL (%)
Electrical	2.5
Visual	4.0

5.3 Electrical criteria

Criteria for electrical characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

a) PURCHASER's incoming inspection should be done within 15 days of PURCHASER receiving the products.

b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data of failure rate, quoting VENDOR's lot number for failed products, if VENDOR demands a report from PURCHASER.

6.2 Inspection procedure

PURCHASER should perform his incoming inspection according to the following procedure.

a) First: Visual inspection should be carried out

b) Second: Electrical and other inspections should be carried out before PURCHASER's manufacturing process is started.

7. Treatment for defective lots and products

Defective lots and defective products which are found in PURCHASER's incoming inspection can be returned to VENDOR with detailed description of failures.
However, if VENDOR does not receive the defective items within 30 days of PURCHASER's incoming inspection, VENDOR is absolved of responsibility for defects.

8. Packing and labeling

a) Dies shall be placed in die tray in order with the top metal surface facing up.

b) A pile consists of five trays and several piles are packed in a package. These piles and packages have printed labels on them as shown below.

Date	
Name	
Lot No.	
Net	
TOSHIBA MADE IN JAPAN	

c) PURCHASER shall return these packing materials to VENDOR at VENDOR's request.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices and are normally fragile and small in size. They therefore, require special handling considerations as follows:

9.1 Chips must be stored under proper conditions to ensure that they are not subjected to a moist and/or contaminated atmosphere that will alter their electrical, physical or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions:

A. Storage temperature: 40°C max
B. Relative humidity: 50% max
C. Clean, dust-free environment

9.2 The user must exercise proper care when handling chips or wafers so as to prevent even the slightest physical damage to the chip.

9.3 During chip-mounting and leads bonding the user must use proper assembly techniques to obtain proper electrical, thermal and mechanical performance.

9.4 After the chip has been mounted and the leads bonded, all necessary procedures must be followed by the user to ensure that these non-hermetic chips are not subjected to a moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environmental factors which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful when handling chips.
In any event, because of the extremely small size and the fragile nature of chips, care should be taken when handling these devices.

10.1 Grounding

a) Bonders, pellet pick-up tools, table tops, trimming and forming tools, sealing equipment and any other equipment used in chip handling should be properly grounded.

b) The operator should be properly grounded.

10.2 In-process handling

a) Assemblies or sub-assemblies of chips should be transported and stored in conductive carriers.

b) All external leads on the assemblies or sub-assemblies should be shorted together.

11. Visual Inspection Criteria

11.1 Visual inspection magnification shall be 40×

11.2 Defects defined:

11.2.1 Thickness

See individual specifications in the technical data sheets.

11.2.2 Chips and cracks

A die shall be rejected if:

Any crack or chip extends for more than a length of 35 μm inside the scribe line (see Figure 1).

11.2.3 Metallization

A die shall be rejected if:

a) more than 25% of the metallization of any bonding pad is missing.

b) there is a short or break which affects electrical characteristics in any lead pattern (see Figure 2).

11.2.4 Glass protection coat

A die shall be rejected if:

The glass protection coat covers more than 25% of any bonding pad.

11.2.5 Attached foreign material

A die shall be rejected if:

a) a die is covered by stains or attached foreign material the area of which is greater than five times the bonding pad area.

b) it exhibits residual ink, stains or attached foreign material which cover more than 20% of any active bonding pad (see Figure 3).

11.2.6 Others

A die shall be rejected if:

a) there are no probe needle scratches on any of the bonding pads.

b) if it has been marked with ink.

11.3 Parameter limits for samples should be applied as necessary

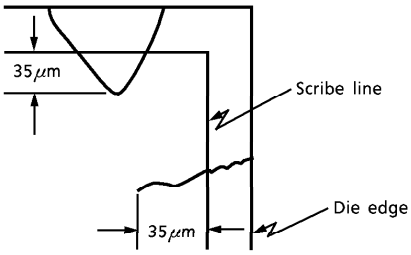


Figure 1

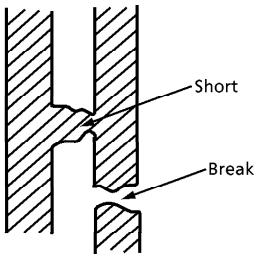


Figure 2 Lead pattern

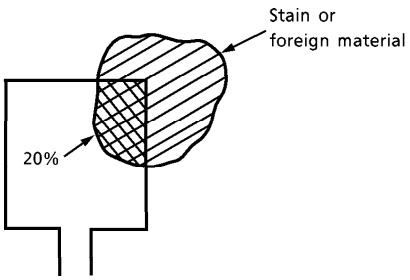
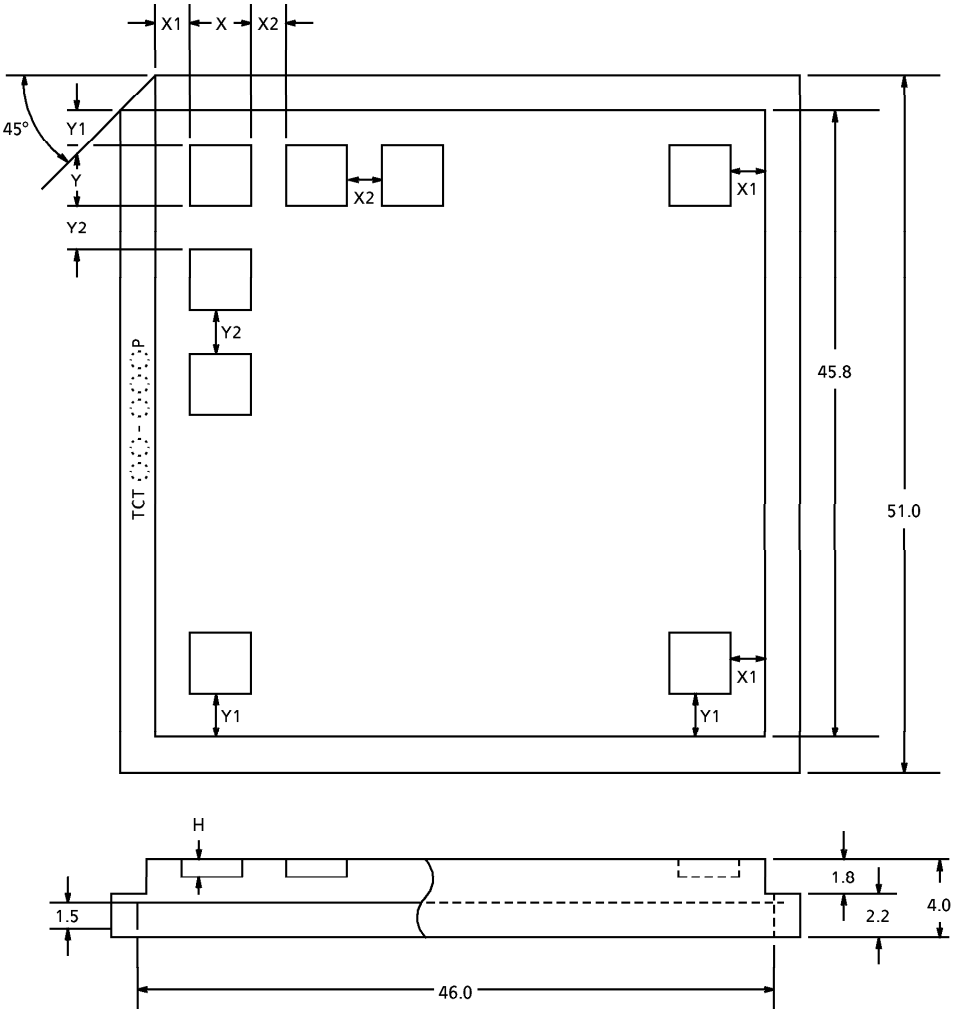


Figure 3

External Dimensions of Chip Tray



Please select a tray name from the table according to the chip size:

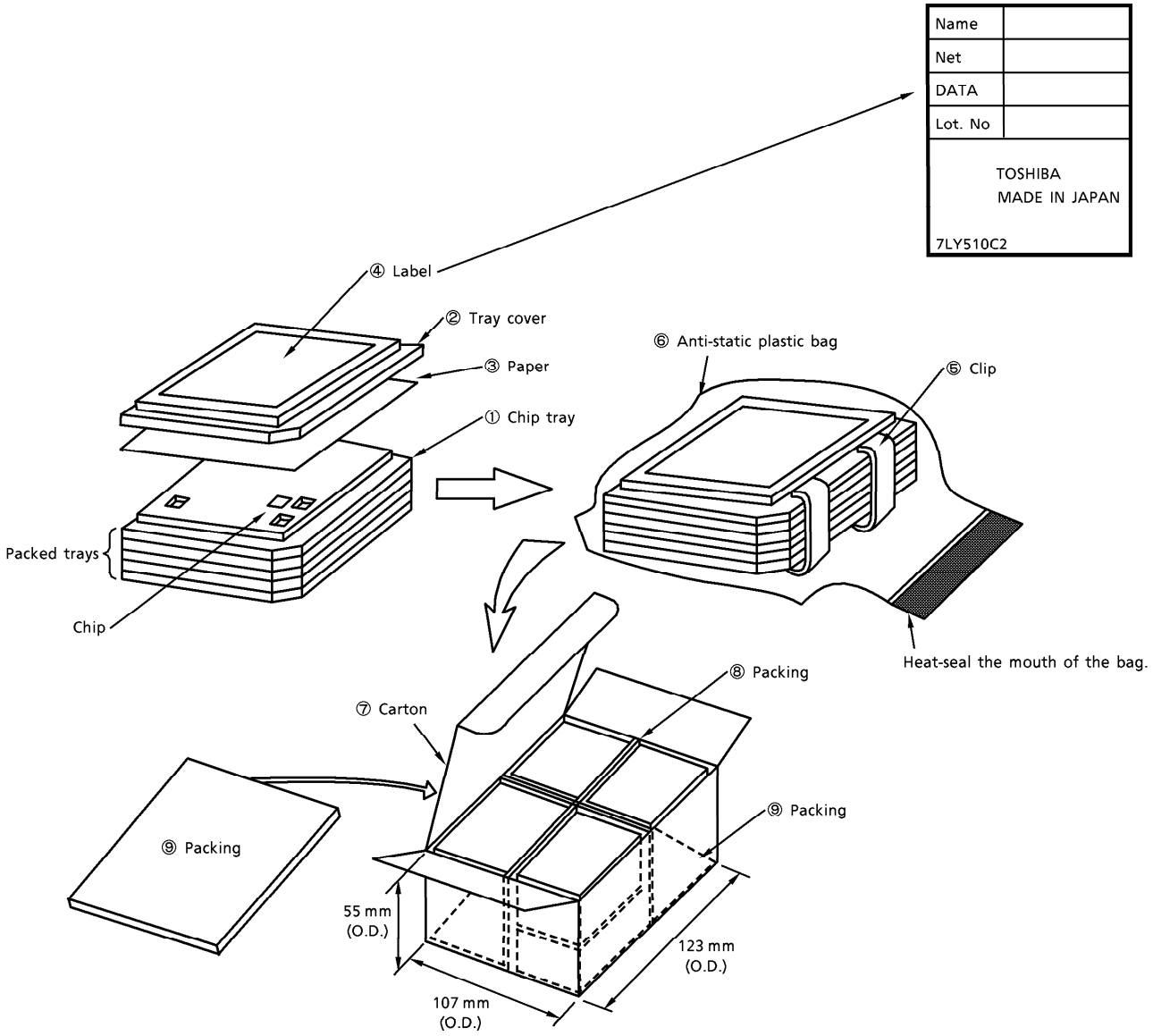
Unit: mm

Tray name	X	Y	H	No. of pockets (pcs)	X1	X2	Y1	Y2
TCT28-060P	2.80	2.80	0.60	10×10 (100)	1.700	1.800	1.700	1.600
TCT33-060P	3.30	3.30	0.60	10×10 (100)	1.900	1.000	1.900	1.000
TCT38-060P	3.80	3.80	0.60	10×10 (100)	1.200	0.600	1.200	0.600
TCT45-060P	4.50	4.50	0.60	7×7 (49)	2.050	1.700	2.050	1.700
TCT53-060P	5.30	5.30	0.60	7×7 (49)	1.350	1.000	1.350	1.000

Tray material:

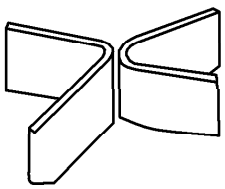
Carbon-bearing polypropylene

Packing Method 1



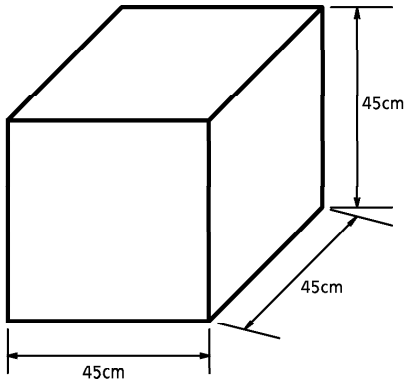
Place eight bags of chip trays in each carton ⑦. Lay one sheet of packing (7UF44F) ⑨ on top before closing the lid of the carton (see the diagram above).

Prepare the packing ⑧ by cutting a sheet of 7UF44F into halves and folding each half in half as shown below; use these halves as inner partitions.



Packing Method 2

Shipping box



- Inner box : Containing 20 boxes
- Weight : Approx. 15 kg (including packing material)
- Material : Corrugated cardboard
- IC contents : 36 × 5 × 8 × 20 = 28.800 pcs